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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,247	11/08/2001	Min Kim	SEC.853	5037

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EXAMINER	
GUERRERO, MARIA F	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/986,247	KIM ET AL.	
	Examiner	Art Unit	
	Maria Guerrero	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-24,26 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-24,26 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Request for reconsideration filed April 28, 2004.

Claims 1-10, 25, and 28 are canceled.

Claims 11-24 and 26-27 are pending.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 11-12 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr (U.S. 5,536,675) in view of Chang et al. (U.S. 6,326,310) and Wu (U.S. 6,165,854).

Bohr teaches a method of manufacturing a trench isolation structure (Abstract). Bohr shows sequentially forming a pad oxide layer and a hard mask layer on a semiconductor substrate, patterning the pad oxide layer and the hard mask layer using photolithography, etching a portion of the semiconductor substrate to form a shallow trench, and forming a thermal oxide layer along inner walls of the semiconductor

substrate that define the shallow trench (Fig. 1, 3A, col. 4, lines 64-67, col. 5, lines 15-20, and 59-65).

Furthermore, Bohr shows the lateral portions of the thermal oxide having a curvilinear section profile at an interface with the upper surface of the semiconductor substrate and a central portion. Bohr shows etching away the central portion of the thermal oxide layer and the semiconductor substrate to extend the shallow trench deeper into the semiconductor substrate (col. 6, lines 10-15, 40-48).

Bohr teaches forming a layer over the deep trench by thermal oxidation (col. 6, lines 40-45), filling the deep trench with a first oxide layer (CVD deposited silicon dioxide or other oxide formation techniques), planarizing the structure, and removing the hard mask pattern (Fig. 2, col. 7, lines 20-27, 40-45, 60-62).

Regarding claims 11-12 and 22-24, Bohr does not specifically show using the hard mask pattern as a mask to extend the shallow trench, forming a spacer along sidewalls of the hard mask pattern and the pad oxide pattern and etching a portion of the semiconductor substrate using the hard mask pattern and the spacer as a mask to form the shallow and deep trenches. However, Bohr teaches various techniques and/or various other materials may be used for the masking and etching of the trenches (col. 7, lines 5-9). In addition, Chang et al. shows forming the spacers along sidewalls of the hard mask pattern and the pad oxide pattern and etching a portion of the semiconductor substrate using the hard mask pattern and the spacers as a mask (Fig. 3-5, col. 4, lines 1-9, 22-30, col. 5, lines 10-30, col. 6, lines 4-10).

Bohr does not specifically show forming a buffer layer over the deep trench. However, Wu teaches forming a plasma-enhance oxide layer as a buffer layer over the entire upper surface in which the trench has been formed (Abstract, Fig. 5, col. 2, lines 37-41, col. 4, lines 14-20).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Bohr reference by including the step of forming the spacer and using the spacer and the hard mask pattern as a mask as taught by Chang et al. and the buffer layer as taught by Wu in order to provide good precision isolation between devices without corner parasitic leakage.

4. Claims 13-14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr (U.S. 5,536,675), Chang et al. (U.S. 6,326,310), and Wu (U.S. 6,165,854) and as applied to claims 11-12 and 22-24 above, and further in view of Benedict et al. (U.S. 5,763,315).

Regarding claims 13-14, the combination of Bohr, Chang et al., and Wu fails to show forming a second oxide layer between the liner and the first oxide layer. However, Benedict et al. shows the step of forming the second oxide layer between the liner and the first oxide layer (Fig. 2B-2E, col. 3, lines 60-63, col. 4, lines 18-21).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to include the step of forming the second oxide layer between the liner and the first oxide layer in the combination of Bohr, Chang et al., and Wu as taught Benedict et al. in order to reduce trap density (Benedict et al., col. 1, lines 59-63).

5. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bohr (U.S. 5,536,675), Chang et al. (U.S. 6,326,310), and Wu (U.S. 6,165,854) as applied to claims 11-12 and 22-24 above, and further in view of Hashimoto et al. (U.S. 6,027,983).

Regarding claims 15-16, the combination of Bohr, Chang et al., and Wu fails to show the silicon layer being monocrystalline, the step of terminating the etching of the semiconductor substrate at an interface between two of the respective of the SOI structure. However, Hashimoto et al. shows forming a deep trench on a semiconductor substrate having a SOI structure. Hashimoto et al. shows the SOI structure comprising a monocrystalline silicon layer, terminating the etching of the semiconductor substrate at an interface between two of the respective layers of the SOI structure (Fig. 7, col. 8, lines 50-55, col. 9, lines 40-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Bohr, Chang et al., and Wu by including the use of the SOI structure as taught by Hashimoto et al. because Bohr suggested that the process could be employed in a variety of applications and in order to improved yield and reliability (Hashimoto et al., col. 2, lines 10-24; Bohr, col. 8, lines 13-20, 32-38).

6. Claims 17-18 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madan (U.S. 5,350,941) in view of Wu (U.S. 6,165,854).

Madan teaches forming a pad oxide layer and a hard mask layer on a flat upper surface of a semiconductor substrate (Fig. 1a-1c, col. 2, lines 37-60). Madan discloses patterning the hard mask layer and forming a thermal oxide layer on a portion of the flat upper surface of the semiconductor substrate (Fig. 1b-1c). Madan teaches the thermal oxide layer having a central portion and lateral potions having the sectional profile of a bird's beak at an interface with the upper surface of the semiconductor substrate (Fig. 1c). Madan shows etching the structure to form a deep trench, removing the central portion of the thermal oxide layer, and leaving the lateral portions of the thermal oxide (Fig. 1e, col. 3, lines 37-55). Madan teaches filling the deep trench with a first oxide layer, etching back (planarizing) the structure, and removing the hard mask pattern (Fig. 1f, col. 4, lines 65-67, col. 4, lines 20-37). Madan discloses forming spacers along sidewall of the hard mask pattern and the pad oxide and employing the spacers as mask to form the deep trench (Fig.1d-1e).

Regarding claims 17-18 and 26-27, Madan does not specifically forming a plasma-enhance oxide layer as a buffer layer over the entire upper surface in which the deep trench has been formed. However, Wu teaches forming a plasma-enhance oxide layer as a buffer layer over the entire upper surface in which the trench has been formed (Abstract, Fig. 5, col. 2, lines 37-41, col. 4, lines 14-20). In addition, Wu discloses filling the trench with a CVD oxide layer and planarizing the structure (Fig. 6, col. 4, lines 25-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Madan's process by including the buffer layer as taught by Wu in order to prevent parasitic leakage (Wu, Abstract).

7. Claims 19-20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Madan (U.S. 5,350,941) and Wu (U.S. 6,165,854) as applied to claims 17-18 and 26-27 above, and further in view of Benedict et al. (U.S. 5,763,315).

Regarding claims 19-20, the combination of Madan and Wu does not specifically show forming liner and a second oxide layer between the liner and the first oxide layer. However, Benedict et al. shows the step of forming the second oxide layer between the liner and the first oxide layer (Fig. 2B-2E, col. 3, lines 60-63, col. 4, lines 18-21).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Madan and Wu by including the step of forming the second oxide layer between the liner and the first oxide layer as taught Benedict et al. in order to reduce trap density (Benedict et al., col. 1, lines 59-63).

8. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Madan (U.S. 5,350,941) and Wu (U.S. 6,165,854) as applied to claims 17-18 and 26-27 above, and further in view of Hashimoto et al. (U.S. 6,027,983).

Regarding claim 21, the combination of Madan and Wu fails to show the silicon layer being monocrystalline, the step of terminating the etching of the semiconductor substrate at an interface between two of the respective of the SOI structure. However, Hashimoto et al. shows forming a deep trench on a semiconductor substrate having a SOI structure. Hashimoto et al. shows the SOI structure comprising a monocrystalline

silicon layer, terminating the etching of the semiconductor substrate at an interface between two of the respective layers of the SOI structure (Fig. 7, col. 8, lines 50-55, col. 9, lines 40-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Madan and Wu by including the use of the SOI structure as taught by Hashimoto et al. in order to improved yield and reliability (Hashimoto et al., col. 2, lines 10-24).

Response to Arguments

9. Applicant's arguments with respect to claims 11-24 and 26-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wu (U.S. 6,020,230) is cited as evidence to show that the step of forming a buffer layer over the trench structure is well known in the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maria Guerrero whose telephone number is 571-272-1837.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Maria Guerrero
Primary Examiner
July 9, 2004